CLAIMS

What is claimed is:

1. A method for controlling a low jitter digital frequency synthesizer, the method comprises:

counting cycles of an input clock to produce an input clock count;

counting cycles of an output clock to produce an output clock count;

when the input clock count reaches a value of D, incrementing a first counter to produce an incremented first count;

when the output clock count reaches a value of M, incrementing a second counter to produce an incremented second count;

periodically taking a snapshot of the incremented first count to produce a snapshot first count;

periodically taking a snapshot of the incremented second count to produce a snapshot second count;

generating an error value based on the snapshot first count and the snapshot second count; and

adjusting a delay line tap value based on the error value.

2. The method of claim 1, wherein the counting cycles of the input clock comprises:

modulo D counting the cycles of the input clock.

3. The method of claim 1, wherein the counting cycles of the output clock comprises:

modulo M counting the cycles of the output clock.

4. The method of claim 1, wherein the periodically taking the snapshot of the incremented first count comprises:

determining whether an increment of the incremented first count is occurring while taking the snapshot;

when the increment of the incremented first count is occurring while taking the snapshot, setting the incremented first count to one when the taking of the snapshot of the incremented first count is complete; and

when the increment of the incremented first count is not occurring while taking the snapshot, setting the incremented first count to zero when the taking of the snapshot of the incremented first count is complete.

5. The method of claim 1, wherein the periodically taking the snapshot of the incremented second count comprises:

determining whether an increment of the incremented second count is occurring while taking the snapshot;

when the increment of the incremented second count is occurring while taking the snapshot, setting the incremented second count to one when the taking of the snapshot of the incremented second count is complete; and

when the increment of the incremented second count is not occurring while taking the snapshot, setting the incremented second count to zero when the taking of the snapshot of the incremented second count is complete.

6. The method of claim 1, wherein the generating the error value comprises:

adding one of the snapshot first count or the snapshot second count with a previous error value to produce an addition error value; and

determining the error value as a difference between the addition error value and another one of the snapshot first value and the snapshot second value.

7. The method of claim 1, wherein the periodically taking the snapshot of the incremented first count and the periodically taking the snapshot of the incremented second count comprise:

within in a period of the periodically taking of the snapshots of the increment first count and the incremented second count:

taking the snapshot of the incremented first count in a first time domain corresponding to the input clock;

when the snapshot of the incremented first count is complete, enabling taking the snapshot of the incremented second count;

when the taking of the snapshot of the incremented second count is enabled, taking the snapshot of the second incremented value in accordance with a second time domain that corresponds to the output clock; and

when the taking of the snapshot of the incremented second count is completed, repeating the taking of the snapshot of the incremented first value and the incremented second value in a subsequent period of the periodically taking of the snapshots.

8. The method of claim 1, wherein the adjusting the delay line tap value based on the error value comprises:

comparing the error value with a previous error value to determine whether sign of the error value has changed with respect to the previous error value; and

when the sign of the error value has changed, determining amount of the adjusting the delay line tap based on the current error value and parameters of the digital frequency synthesizer.

9. The method of claim 1, wherein the adjusting the delay line tap value based on the error value comprises:

comparing the error value with a previous error value to determine whether magnitude of the error value has increased with respect to the previous error value; and

when the magnitude of the error value has increased, determining amount of the adjusting the delay line tap based on the current error value and parameters of the digital frequency synthesizer.

10. An apparatus for controlling a low jitter digital frequency synthesizer, the apparatus comprises:

a processing module; and

memory operably coupled to the processing module, wherein the memory stores operational instructions that cause the processing module to:

count cycles of an input clock to produce an input clock count;

count cycles of an output clock to produce an output clock count;

when the input clock count reaches a value of D, increment a first counter to produce an incremented first count;

when the output clock count reaches a value of M, increment a second counter to produce an incremented second count;

periodically take a snapshot of the incremented first count to produce a snapshot first count;

periodically take a snapshot of the incremented second count to produce a snapshot second count;

generate an error value based on the snapshot first count and the snapshot second count; and

adjust a delay line tap value based on the error value.

11. The apparatus of claim 10, wherein the memory further stores operational instructions that cause the processing module to count cycles of the input clock by:

modulo D counting the cycles of the input clock.

12. The apparatus of claim 10, wherein the memory further stores operational instructions that cause the processing module to count cycles of the output clock by:

modulo M counting the cycles of the output clock.

13. The apparatus of claim 10, wherein the memory further stores operational instructions that cause the processing module to periodically take the snapshot of the incremented first count by:

determining whether an increment of the incremented first count is occurring while taking the snapshot;

when the increment of the incremented first count is occurring while taking the snapshot, setting the incremented first count to one when the taking of the snapshot of the incremented first count is complete; and

when the increment of the incremented first count is not occurring while taking the snapshot, setting the incremented first count to zero when the taking of the snapshot of the incremented first count is complete.

14. The apparatus of claim 10, wherein the memory further stores operational instructions that cause the processing module to periodically take the snapshot of the incremented second count by:

determining whether an increment of the incremented second count is occurring while taking the snapshot;

when the increment of the incremented second count is occurring while taking the snapshot, setting the incremented second count to one when the taking of the snapshot of the incremented second count is complete; and

when the increment of the incremented second count is not occurring while taking the snapshot, setting the incremented second count to zero when the taking of the snapshot of the incremented second count is complete.

15. The apparatus of claim 10, wherein the memory further stores operational instructions that cause the processing module to generate the error value by:

adding one of the snapshot first count or the snapshot second count with a previous error value to produce an addition error value; and

determining the error value as a difference between the addition error value and another one of the snapshot first value and the snapshot second value.

16. The apparatus of claim 10, wherein the memory further stores operational instructions that cause the processing module to periodically take the snapshot of the incremented first count and the periodically take the snapshot of the incremented second count by:

within in a period of the periodically taking of the snapshots of the increment first count and the incremented second count:

taking the snapshot of the incremented first count in a first time domain corresponding to the input clock;

when the snapshot of the incremented first count is complete, enabling taking the snapshot of the incremented second count;

when the taking of the snapshot of the incremented second count is enabled, taking the snapshot of the second incremented value in accordance with a second time domain that corresponds to the output clock; and

when the taking of the snapshot of the incremented second count is completed, repeating the taking of the snapshot of the incremented first value and the incremented second value in a subsequent period of the periodically taking of the snapshots.

17. The apparatus of claim 10, wherein the memory further stores operational instructions that cause the processing

module to adjust the delay line tap value based on the error value by:

comparing the error value with a previous error value to determine whether sign of the error value has changed with respect to the previous error value; and

when the sign of the error value has changed, determining amount of the adjusting the delay line tap based on the current error value and parameters of the digital frequency synthesizer.

18. The apparatus of claim 10, wherein the memory further stores operational instructions that cause the processing module to adjust the delay line tap value based on the error value by:

comparing the error value with a previous error value to determine whether magnitude of the error value has increased with respect to the previous error value; and

when the magnitude of the error value has increased, determining amount of the adjusting the delay line tap based on the current error value and parameters of the digital frequency synthesizer.

19. A low jitter digital frequency synthesizer comprises:

a first counter module operably coupled to count intervals of M cycles of an input clock of the low jitter digital frequency synthesizer to produce a first count;

a second counter module operably coupled to count intervals of D cycles of an output clock of the low jitter digital frequency synthesizer to produce a second count, wherein a rate of the output clock corresponds to M/D times a rate of the input clock;

a snapshot module operably coupled to periodically take a snapshot of the first count to produce a first snapshot and of the second count to produce a second snapshot;

an error value generation module operably coupled to generate an error value based on the first and second snapshots; and

a tapped delay line module operably coupled to produce the output clock based on the error value.

20. The low jitter digital frequency synthesizer of claim 19, wherein the first counter module comprises:

a modulo M counter operably coupled to modulo M count cycles of the input clock to produce a first modulo count; and

a first incrementing counter operably coupled to increment the first count based on a wrap-around of the first modulo count.

21. The low jitter digital frequency synthesizer of claim 19, wherein the first counter module comprises:

a modulo D counter operably coupled to modulo D count cycles of the output clock to produce a second modulo count; and

a second incrementing counter operably coupled to increment the second count based on a wrap-around of the second modulo count.

22. The low jitter digital frequency synthesizer of claim 19, wherein the snapshot module comprises:

a reset module operably coupled to:

determining whether an increase of the first count is occurring while taking the snapshot of the first count;

when the increase of the first count is occurring while taking the snapshot of the first count, setting the first count to one when the taking of the snapshot of the first count is complete; and

when the increase of the first count is not occurring while taking the snapshot of the first count, setting the

first count to zero when the taking of the snapshot of the first count is complete.

23. The low jitter digital frequency synthesizer of claim 19, wherein the snapshot module comprises:

a reset module operably coupled to:

determining whether an increase of the second count is occurring while taking the snapshot of the second count;

when the increase of the second count is occurring while taking the snapshot of the second count, setting the second count to one when the taking of the snapshot of the second count is complete; and

when the increase of the second count is not occurring while taking the snapshot of the second count, setting the second count to zero when the taking of the snapshot of the second count is complete.

24. The low jitter digital frequency synthesizer of claim 19, wherein error value generation module further functions to:

add one of the first snapshot or the second snapshot to a previous error value to produce an addition error value; and

determine the error value as a difference between the addition error value and another one of the first snapshot and the second snapshot.

25. The low jitter digital frequency synthesizer of claim 19, wherein the snapshot module further functions to:

within in a period of the periodically taking of the snapshots of the first count and the second count:

take the snapshot of the first count in a first time domain corresponding to the input clock;

when the snapshot of the first count is complete, enable taking the snapshot of the second count;

when the taking of the snapshot of the second count is enabled, take the snapshot of the second value in accordance with a second time domain that corresponds to the output clock; and

when the taking of the snapshot of the second count is completed, repeat the taking of the snapshot of the first value and the second value in a subsequent period of the periodically taking of the snapshots.

26. The low jitter digital frequency synthesizer of claim 19, wherein the tapped delay line module comprises a control module operable coupled to adjust the delay line tap value based on the error value by:

comparing the error value with a previous error value to determine whether sign of the error value has changed with respect to the previous error value; and

when the sign of the error value has changed, determining amount of the adjusting the tapped delay line module based on the current error value and parameters of the digital frequency synthesizer.

27. The low jitter digital frequency synthesizer of claim 19, wherein the tapped delay line module comprises a control module operable coupled to adjust the delay line tap value based on the error value by:

comparing the error value with a previous error value to determine whether magnitude of the error value has increased with respect to the previous error value; and

when the magnitude of the error value has increased, determining amount of the adjusting the tapped delay line module based on the current error value and parameters of the digital frequency synthesizer.

28. A programmable logic device comprises:

a programmable logic fabric;

memory operably coupled to the programmable logic fabric;

an input/output section operably coupled to the programmable logic fabric and to the memory. wherein the input/output section includes a low jitter digital frequency synthesizer that includes:

a first counter module operably coupled to count intervals of M cycles of an input clock of the low jitter digital frequency synthesizer to produce a first count;

a second counter module operably coupled to count intervals of D cycles of an output clock of the low jitter digital frequency synthesizer to produce a second count, wherein a rate of the output clock corresponds to M/D times a rate of the input clock;

a snapshot module operably coupled to periodically take a snapshot of the first count to produce a first snapshot and of the second count to produce a second snapshot;

an error value generation module operably coupled to generate an error value based on the first and second snapshots; and

a tapped delay line module operably coupled to produce the output clock based on the error value.

29. The programmable logic device of claim 28, wherein the first counter module comprises:

a modulo M counter operably coupled to modulo M count cycles of the input clock to produce a first modulo count; and

a first incrementing counter operably coupled to increment the first count based on a wrap-around of the first modulo count.

30. The programmable logic device of claim 28, wherein the first counter module comprises:

a modulo D counter operably coupled to modulo D count cycles of the output clock to produce a second modulo count; and

a second incrementing counter operably coupled to increment the second count based on a wrap-around of the second modulo count.

31. The programmable logic device of claim 28, wherein the snapshot module comprises:

a reset module operably coupled to:

determining whether an increase of the first count is occurring while taking the snapshot of the first count;

when the increase of the first count is occurring while taking the snapshot of the first count, setting the first count to one when the taking of the snapshot of the first count is complete; and

when the increase of the first count is not occurring while taking the snapshot of the first count, setting the first count to zero when the taking of the snapshot of the first count is complete.

32. The programmable logic device of claim 28, wherein the snapshot module comprises:

a reset module operably coupled to:

determining whether an increase of the second count is occurring while taking the snapshot of the second count;

when the increase of the second count is occurring while taking the snapshot of the second count, setting the second count to one when the taking of the snapshot of the second count is complete; and

when the increase of the second count is not occurring while taking the snapshot of the second count, setting the second count to zero when the taking of the snapshot of the second count is complete.

33. The programmable logic device of claim 28, wherein error value generation module further functions to:

add one of the first snapshot or the second snapshot to a previous error value to produce an addition error value; and

determine the error value as a difference between the addition error value and another one of the first snapshot and the second snapshot.

34. The programmable logic device of claim 28, wherein the snapshot module further functions to:

within in a period of the periodically taking of the snapshots of the first count and the second count:

take the snapshot of the first count in a first time domain corresponding to the input clock;

when the snapshot of the first count is complete, enable taking the snapshot of the second count;

when the taking of the snapshot of the second count is enabled, take the snapshot of the second value in accordance with a second time domain that corresponds to the output clock; and

when the taking of the snapshot of the second count is completed, repeat the taking of the snapshot of the first value and the second value in a subsequent period of the periodically taking of the snapshots.

35. The programmable logic device of claim 28, wherein the tapped delay line module comprises a control module operable coupled to adjust the delay line tap value based on the error value by:

comparing the error value with a previous error value to determine whether sign of the error value has changed with respect to the previous error value; and

when the sign of the error value has changed, determining amount of the adjusting the tapped delay line module based on the current error value and parameters of the digital frequency synthesizer.

36. The programmable logic device of claim 28, wherein the tapped delay line module comprises a control module operable coupled to adjust the delay line tap value based on the error value by:

comparing the error value with a previous error value to determine whether magnitude of the error value has increased with respect to the previous error value; and

when the magnitude of the error value has increased, determining amount of the adjusting the tapped delay line module based on the current error value and parameters of the digital frequency synthesizer.